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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,310	02/24/2004	Leonard Forbes	400.264US01	9673

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,310	FORBES, LEONARD	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) *41-71* is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,13 and 14* is/are allowed.

6)☒ Claim(s) *4-12,15-30 and 32-40* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 07/15/2005 has been entered.

Specification

2. **Claim 4** is objected to because of the following informalities: Claim 4 recites: "the select gate" which lacks a clear antecedent basis. It is clear from the detailed description that the select gate derives an antecedent from select gate (610), and not from the "a select gate memory cell (610)" as claimed.

Appropriate correction is required.

3. **Claims 1, 12, 13, 14, 15, 16, 17, 18, 25, 27, and 40** are objected to because of the following informalities: Each of these claims either recites: "memory array formed on a substrate" or "forming two raised areas on a substrate"; however, it is clear from the detailed description that the respective elements are formed in a substrate (paragraph [0049]: "In creating the vertical NOR architecture memory cell structure 604 a trench 630 is formed in a substrate

608", paragraph [0071]: "a series of substrate pillars 828 are formed in a substrate 808 with trenches 830 located between them").

Appropriate correction is required.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "on a substrate" and "depositing additional substrate material on the substrate" in "forming two pillars on a substrate further comprises depositing additional substrate material on the substrate to form the two pillars" of **claim 18** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Allowable Subject Matter

5. The indicated allowability of claims 4-12,15-30, and 32-40 is withdrawn in view of the newly discovered reference(s) to Yamazaki et al. U.S. Patent 5,888,868, cited by Applicant, in view of Sakui et al. U.S. Patent Application Publication 20010038118 or Takahashi et al. U.S. Patent Application Publication 20030209767 (the '767 reference). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 4-12,15-30 and 32-40** are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki et al. U.S. Patent 5,888,868 (the '868 reference, cited by Applicant) in view of Sakui et al. U.S. Patent Application Publication 20010038118 (the '118 reference).

The '868 reference discloses in the second embodiment, namely Figs. 1, 3, and 8A-8F, a memory cell structure including at least a memory cell having a memory storage layer as claimed but fails to teach that the memory storage layer comprises a nitride (nitride read only memory – NROM).

Specifically, in reference to **claims 4-5, 7, 15-18, 20-28, 34-37, and 40**, the reference discloses a memory cell structure and a method of forming thereof, comprising:

a substrate (no number, column 8, lines 43-47), comprising a plurality of raised areas or pillars (generally indicated at 31 and 32, Fig. 8A) and associated intervening trenches therebetween; and

a plurality of memory cell structures, each memory cell structure comprising:

a memory cell, wherein the memory cell (generally indicated at 21/24/25/27, Figs. 8A-8F) is formed vertically on a first sidewall of a trench; and

a select gate (generally indicated at 21/27), wherein the select gate is formed vertically on a second sidewall of the trench and wherein the memory cell is coupled to the select gate by source/drain regions ("impurity regions" 29, column 11, lines 20-27) at the bottom of the trench.

However, as noted above, the memory cell (21/24/25/27) having the memory storage layer (24), which is formed from conductive film 22 (paragraph bridging columns 10 and 11). Therefore, the reference does not disclose that the memory storage layer comprises a nitride as claimed and therefore does not disclose an NROM as claimed.

The '118 reference, in also disclosing a memory cell structure and a method of forming thereof, comprising a substrate (13, for example Fig. 3B) including a plurality of raised areas or pillars and associated intervening trenches therebetween, a plurality of memory cell structures (MT) formed vertically on a first sidewall of a trench of the intervening trenches, each memory cell structure comprising a memory storage layer indicated generally at FG, teaches that the memory storage layer could be a conductive layer (FG) or a nitride layer (paragraph [0102]), thereby teaching that the two materials are art equivalents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '868 reference's device and inherent method of forming the

device such that the memory storage layer (24) comprises a nitride as claimed. One would have been motivated to make such a change in view of the teachings in the '118 reference that such a change was possible because of the suitability, availability, and the art-equivalency of the various materials.

Referring to **claims 6, 8, 29-30, 32-33, and 38**, although the '868 reference does not disclose details as claimed for word lines, bit lines, and select lines as claimed, word lines, bit lines, and select lines as claimed at the time the invention was made were normally arranged as claimed and as detailed by, for example, Fig. 1 of the '118 reference, therefore such arrangements would have been obvious to one of ordinary skill in the art.

Referring to **claims 8, 19, 25, and 38,** the references further disclose that forming a source/drain region at the bottom of the associated intervening trench further comprises forming source/drain regions on the top of the two raised areas.

Referring to **claims 9 and 39**, the references further disclose that the plurality of NROM memory cell structures are formed into rows and columns such that each trench contains an NROM memory cell structure and where the NROM memory cell and select gate of each NROM memory cell structure of each row is arranged in an alternating pattern, such that each pillar of the row has either two select gates or two NROM memory cells formed on opposing sidewalls (the '868 reference, Figs. 3 and 8).

Referring to **claims 10-12 and 26**, the references further disclose that the plurality of NROM memory cell structures are formed into rows and columns and an isolation region (15) is formed between adjacent rows of NROM memory cell structures (the '868 reference, Figs. 3, 5A-B, and 8).

7. **Claims 4-12,15-30 and 32-40** are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki et al. U.S. Patent 5,888,868 (the '868 reference, cited by Applicant) in view of Takahashi et al. U.S. Patent Application Publication 20030209767 (the '767 reference).

The '868 reference discloses in the second embodiment, namely Figs. 1, 3, and 8A-8F, a memory cell structure including at least a memory cell having a memory storage layer as claimed but fails to teach that the memory storage layer comprises a nitride (nitride read only memory – NROM).

Specifically, in reference to **claims 4-5, 7, 15-18, 20-28, 34-37, and 40**, the reference discloses a memory cell structure and a method of forming thereof, comprising:

a substrate (no number, column 8, lines 43-47), comprising a plurality of raised areas or pillars (generally indicated at 31 and 32, Fig. 8A) and associated intervening trenches therebetween; and

a plurality of memory cell structures, each memory cell structure comprising:

a memory cell, wherein the memory cell (generally indicated at 21/24/25/27, Figs. 8A-8F) is formed vertically on a first sidewall of a trench; and

a select gate (generally indicated at 21/27), wherein the select gate is formed vertically on a second sidewall of the trench and wherein the memory cell is coupled to the select gate by source/drain regions ("impurity regions" 29, column 11, lines 20-27) at the bottom of the trench.

However, as noted above, the memory cell (21/24/25/27) having the memory storage layer (24), which is formed from conductive film 22 (paragraph bridging columns 10 and 11).

Therefore, the reference does not disclose that the memory storage layer comprises a nitride as claimed and therefore does not disclose an NROM as claimed.

The '767 reference, in also disclosing a memory cell structure and a method of forming thereof, comprising a substrate (10, for example Fig. 2B) including a plurality of raised areas or pillars and associated intervening trenches (16) therebetween, a plurality of memory cell structures formed vertically on a first sidewall of a trench of the intervening trenches, each memory cell structure comprising a memory storage layer ONO 28 (paragraphs [0045] and [0046]), teaches that the memory storage layer formed of a nitride layer in order to utilize simple fabrication and high integration (paragraph [0004]: "As a nonvolatile semiconductor memory device which has a simple structure and can be easily higher-integrated is proposed a nonvolatile semiconductor memory device comprised of a single-gate memory cell transistor by using an insulating film as a charge storage layer").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '868 reference's device and inherent method of forming the device such that the memory storage layer (24) comprises a nitride as claimed. One would have been motivated to make such a change in view of the teachings in the '767 reference that such a change provides simple fabrication and high integration.

Referring to **claims 6, 8, 29-30, 32-33, and 38**, although the '868 reference does not disclose details as claimed for word lines, bit lines, and select lines as claimed, word lines, bit lines, and select lines as claimed at the time the invention was made were normally arranged as claimed and as detailed by, for example, Fig. 1 of the '118 reference, therefore such arrangements would have been obvious to one of ordinary skill in the art.

Referring to **claims 8, 19, 25, and 38,** the references further disclose that forming a source/drain region at the bottom of the associated intervening trench further comprises forming source/drain regions on the top of the two raised areas.

Referring to **claims 9 and 39**, the references further disclose that the plurality of NROM memory cell structures are formed into rows and columns such that each trench contains an NROM memory cell structure and where the NROM memory cell and select gate of each NROM memory cell structure of each row is arranged in an alternating pattern, such that each pillar of the row has either two select gates or two NROM memory cells formed on opposing sidewalls (the '868 reference, Figs. 3 and 8).

Referring to **claims 10-12 and 26**, the references further disclose that the plurality of NROM memory cell structures are formed into rows and columns and an isolation region (15) is formed between adjacent rows of NROM memory cell structures (the '868 reference, Figs. 3, 5A-B, and 8).

Allowable Subject Matter

8. Claims 1-3 and 13-14 are allowable over the prior art of record.

Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a memory structure and a method of forming thereof with all exclusive limitations as recited in claims 1, 13, 14, and 31, characterized in that the memory structure comprises a NOR architecture NROM structure.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
September 12, 2005